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Question Paper Code : 60514

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2026.

Sixth/Seventh Semester

Electronics and Communication Engineering

EC 8095 — VLSI DESIGN

(Common to: Electrical and Electronics Engineering/Electronics and Instrumentation Engineering/Electronics and Telecommunication Engineering/Instrumentation and Control Engineering/Robotics and Automation)

(Regulations 2017)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Realize the 2:1 multiplexer using transmission gates.
2. What is threshold voltage?
3. Differentiate static and dynamic power.
4. Realize the AND gate using pass transistor logic.
5. Differentiate static and dynamic latch.
6. What is the principle of metastability?
7. What is memory peripheral circuitry?
8. Name the arithmetic and logic unit blocks.
9. What are the advantages of Adhoc testing methods?
10. What is IDDQ testing?

PART B — ($5 \times 13 = 65$ marks)

11. (a) Derive the DC transfer characteristics of a CMOS inverter and determine noise margins.

Or

- (b) Discuss the long-channel MOS I-V characteristics for different regions of operation.

12. (a) Simplify the function $F(x, y, z) = \sum m(0, 1, 6, 7)$ using K-map and realize it using

- (i) CMOS logic
- (ii) Ratioed logic
- (iii) Dynamic logic
- (iv) Domino logic (3+3+3+4)

Or

- (b) (i) Compare CPL, DCVSPG, and DPL logic styles. (7)
(ii) Discuss low-power design techniques in combinational circuits. (6)

13. (a) Analyze dynamic latches and registers and discuss the charge retention capability in dynamic register.

Or

- (b) (i) Analyze timing violations in synchronous circuits. (6)
(ii) Construct a Schmitt trigger using MOS transistor and explain the operation. (7)

14. (a) Explain memory architectures and building blocks in subsystem design.

Or

- (b) Design a ripple carry adder and compare carry look-ahead adder with ripple carry adder.

15. (a) Construct FPGA architecture using logic blocks and interconnects.

Or

- (b) (i) Discuss manufacturability issues and their impact on yield. (7)
(ii) Determine testability improvements using design-for-testability techniques. (6)

PART C — (1 × 15 = 15 marks)

16. (a) (i) Evaluate the impact of parasitic capacitances on switching performance. (7)
- (ii) Analyze charge sharing effect in dynamic logic circuits. Provide solution to overcome the charge sharing effect. (8)

Or

- (b) (i) Analyze boundary scan technique for testing integrated circuits and compare scan design and BIST. (8)
- (ii) Apply pipelining to a given function $y = \log[(a_n * b_n) + c_n]$ and compute throughput improvement for $n = 1, 2, 3$. (7)
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